IN THE CLAIMS

Please cancel claim 12.

Please amend claims 1, 31, 34, and 35 as follows:

1. (Currently Amended) A random access memory, comprising:

an array of memory cells;

a memory configured to receive data from the array of memory cells;

a bypass circuit configured to receive a column address strobe latency select signal and the data from the array of memory cells and to bypass the memory, the bypass circuit configured to tri-state an output if the column address strobe latency select signal indicates a column address strobe latency value greater than one; and

a circuit configured to receive the column address strobe latency select signal and to select between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on ~~a~~ the column address strobe latency select signal.

2. (Previously Presented) The random access memory of claim 1, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency select signal indicates a column address strobe latency value of one.

3. (Previously Presented) The random access memory of claim 1, wherein the circuit is configured to receive the data from the memory and provide the first output signals if the column address strobe latency select signal indicates a column address strobe latency value of greater than one.

4. (Original) The random access memory of claim 1, wherein the circuit comprises a first circuit configured to receive first rise and fall signals to serialize the data from the memory.

5. (Original) The random access memory of claim 4, wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle.

6. (Original) The random access memory of claim 4, wherein the circuit comprises a second circuit configured to receive second rise and fall signals to serialize the data from the bypass circuit.

7. (Original) The random access memory of claim 6, wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle and the second rise and fall signals during the first clock cycle.

8. (Previously Presented) The random access memory of claim 6, wherein the circuit comprises a multiplexer configured to select between serialized data from the first circuit and serialized data from the second circuit based on the column address strobe latency select signal.

9. (Original) The random access memory of claim 1, wherein the circuit comprises a rise and fall circuit configured to receive first rise and fall signals to serialize the data from the memory and to receive second rise and fall signals to serialize the data from the bypass circuit.

10. (Previously Presented) The random access memory of claim 9, wherein the circuit is configured to select between providing the first rise and fall signals and providing the second rise and fall signals based on the column address strobe latency select signal.

11. (Original) The random access memory of claim 10, wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read

command that is initiated by a first edge of the first clock cycle and the second rise and fall signals during the first clock cycle.

12. (Cancelled)

13. (Original) The random access memory of claim 1, wherein the memory comprises a first in/first out memory.

14. (Original) The random access memory of claim 1, wherein the random access memory is a low power synchronous dynamic random access memory.

15. (Original) The random access memory of claim 1, wherein the random access memory is a double data rate-I synchronous dynamic random access memory.

16. (Original) The random access memory of claim 1, wherein the random access memory is a double data rate-II synchronous dynamic random access memory.

17. (Original) A random access memory, comprising:

a first in/first out memory;

a bypass circuit that bypasses the first in/first out memory; and

a control circuit configured to provide first signals and second signals, wherein the first signals latch data from the first in/first out memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one.

18. (Previously Presented) The random access memory of claim 17, wherein the control circuit comprises a clock signal multiplexer configured to select between providing the first signals and the second signals based on a column address strobe latency select signal.

19. (Original) The random access memory of claim 17, comprising a rise/fall circuit configured to receive the first signals and the second signals to provide one data bit at a time.

20. (Original) The random access memory of claim 19, wherein the control circuit is configured to provide the first signals comprising a first rise signal and a first fall signal that is the inverse of the first rise signal and the second signals comprising a second rise signal and a second fall signal that is the inverse of the second rise signal.

21. (Original) The random access memory of claim 20, wherein the rise/fall circuit is configured to provide a first data bit as output on a rising edge of the first rise signal and a second data bit as output on a rising edge of the first fall signal.

22. (Original) The random access memory of claim 19, comprising a data delay circuit electrically coupled to the rise/fall circuit and configured to adjust output timing of the data.

23. (Original) The random access memory of claim 22, comprising an off chip driver configured to pass data from the data delay circuit to a data pad.

24. (Original) The random access memory of claim 17, wherein the bypass comprises a tri-state output that is set to a high impedance state for the column address strobe latency of greater than one.

25. (Previously Presented) A random access memory, comprising:

a memory circuit;

a bypass circuit configured to bypass the memory circuit;

a first rise/fall circuit configured to receive data from the memory circuit to provide a first output signal;

a second rise/fall circuit configured to receive data from the bypass circuit to provide a second output signal; and

a multiplexer configured to select between the first output signal and the second output signal based on a column address strobe latency select signal.

26. (Previously Presented) The random access memory of claim 25, wherein the multiplexer selects the first output signal if the column address strobe latency signal indicates the column address strobe latency is greater than one and the second output signal if the column address strobe latency select signal indicates the column address strobe latency is one.

27. (Original) The random access memory of claim 25, comprising a controller configured to provide a first signal and a second signal to the first rise/fall circuit and a third signal and a fourth signal to the second rise/fall circuit.

28. (Original) The random access memory of claim 27, wherein the controller is configured to create the first signal and the second signal from a clock signal and the third signal and the fourth signal from the inverted clock signal.

29. (Original) The random access memory of claim 28, wherein the first rise/fall circuit outputs a first data bit on a rising edge of the first signal and a second data bit on a rising edge of the second signal.

30. (Original) The random access memory of claim 28, wherein the second rise/fall circuit outputs a first data bit on a rising edge of the third signal and a second data bit on a rising edge of the fourth signal.

31. (Currently Amended) A random access memory comprising:

means for storing data read from an array of memory cells;

means for receiving the data read from the array of memory cells to bypass the means for storing data, the means for receiving the data configured to tri-state an output if column address strobe latency is greater than one;

means for retrieving the data from the means for storing the data if the column address strobe latency is greater than one;

means for retrieving the data from the means for receiving the data if the column address strobe latency is one.

32. (Original) The random access memory of claim 31, wherein the means for storing data comprises a first in/first out memory.

33. (Original) The random access memory of claim 31, comprising means for serializing the data retrieved from the means for storing and the means for receiving to provide serial data bit output signals.

34. (Currently Amended) A method for reading data from a random access memory in a column address strobe latency of one, comprising:

initiating a read command on a first edge of a clock cycle;

receiving data read from the array of memory cells in a bypass circuit during the clock cycle, the bypass circuit including a tri-state output configured to be in a high impedance state in response to a column address strobe latency greater than one;

receiving data read from the array of memory cells in a first in/first out memory; and

retrieving the data from the bypass circuit during the clock cycle.

35. (Currently Amended) The method of claim 34, comprising bypassing first in/first out memory cells used to provide data if the column address strobe latency is ~~greater than~~ one.

36. (Original) The method of claim 34, comprising:

generating an inverted clock signal from a data clock signal to retrieve the data from the bypass circuit.

37. (Original) The method of claim 36, comprising:

generating a first signal and a second signal from the inverted clock signal to retrieve the data from the bypass circuit.

38. (Original) The method of claim 37, comprising outputting a first data bit on a rising edge of the first signal and a second data bit on a rising edge of the second signal.